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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,997	11/13/2001	Kenji Orita	740819-617	6386

22204 7590 12/03/2003

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EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,997	ORITA ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-15* is/are allowed.

6)☒ Claim(s) *16-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/389,024.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Reissue Applications

1. The reissue oath/declaration filed with this application is defective because it fails to comply with MPEP.1414. Specifically, the oath fails to identify the priority documents.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 16, 17, 18, 19, 20, 21, 22, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this present application in view of Shih et al. (US '320) and Isamu et al. (Japan 02257679) (reference previously cited in parent case).

The applicant's admitted prior art teaches a method for fabricating a semiconductor device, comprising the steps of (see col. 1, line 5 to col. 2, line 61 of the Background and figure 10 of the patent no. 6,117,700):

a) forming a semiconductor layer 104 of a group III nitride containing a dopant over a substrate 101, wherein the dopant includes magnesium (Mg), zinc (Zn), calcium (Ca), strontium (Sr), and beryllium (Be);

b) exposing the semiconductor layer to plasma at temperature, thereby making the conductivity type of semiconductor layer p-type;

c) after step b) forming a p-side electrode out of a metal on the semiconductor layer.

The applicant's admitted prior art teaches performing plasma heating after the formation of the semiconductor layer 104 of a group III nitride containing a dopant, but fails to teach that the plasma heating is done in the presence nitrogen and that the plasma is generated by RF as recited in present claims 16 and 20.

Shih teaches a method of forming a semiconductor layer in which a semiconductor layer of a group III nitride containing a dopant is annealed by nitrogen plasma that is generated by RF. See the abstract.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to anneal the semiconductor layer 104 of a group III nitride containing a dopant by nitrogen plasma that is generated by RF in the method of the applicant's admitted prior art because in doing so the unwanted defects caused by high temperature process are prevented. See the abstract.

The applicant's admitted prior art teaches exposing the semiconductor layer to plasma for activating the p-type dopant at a temperature, but fails to teach annealing temperature range of 600°C or less as recited in present claims 18 and 22.

Isamu teaches a method of making a gallium nitride compound semiconductor light-emitting device in which a group III nitride containing a dopant is exposed to heat at a temperature of 600°C or less. See the English abstract and figure 5.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to expose the group III nitride containing a dopant to heat

at temperature of 600°C or less in the method of the applicant's admitted prior art because in doing so the optical characteristics of the device are improved without changing electrical characteristics. See the English abstract.

The applicant's admitted prior art teaches exposing the semiconductor layer to plasma for activating the p-type dopant before the formation of the p-side but fails to teach exposing the semiconductor layer to plasma after the formation of the electrode as recited in present claim 23.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to expose the semiconductor layer to plasma for activating the p-type dopant after the formation of the p-side electrode because in the absence of new or unexpected results, the mere reversal of the order of performing process steps has been held to be prima facie obvious. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

3. Claims 25, 26, 27, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this present application in view of Shih et al. (US '320) and Isamu et al. (Japan 02257679).

The applicant's admitted prior art teaches a method for fabricating a semiconductor device, comprising the steps of (see col. 1, line 5 to col. 2, line 61 of the Background and figure 10 of the patent no. 6,117,700):

a) forming a semiconductor layer 104 of a group III nitride containing a dopant over a substrate 101, wherein the dopant includes magnesium (Mg), zinc (Zn), calcium (Ca), strontium (Sr), and beryllium (Be);

b) exposing the semiconductor layer to plasma at temperature, thereby making the conductivity type of semiconductor layer p-type; and

c) after step b) forming a p-side electrode out of a metal on the semiconductor layer, wherein the metal includes nickel and gold.

The applicant's admitted prior art teaches performing plasma heating after the formation of the semiconductor layer 104 of a group III nitride containing a dopant, but fails to teach that the plasma heating is done in the presence nitrogen and that the plasma is generated by RF as recited in present claims 25 and 32.

Shih teaches a method of forming a semiconductor layer in which a semiconductor layer of a group III nitride containing a dopant is annealed by nitrogen plasma that is generated by RF. See the abstract.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to anneal the semiconductor layer 104 of a group III nitride containing a dopant by nitrogen plasma that is generated by RF in the method of the applicant's admitted prior art because in doing so the unwanted defects caused by high temperature process are prevented. See the abstract.

The applicant's admitted prior art teaches exposing the semiconductor layer to plasma for activating the p-type dopant at a temperature, but fails to teach annealing temperature range of 600°C or less as recited in present claim 26.

Isamu teaches a method of making a gallium nitride compound semiconductor light-emitting device in which a group III nitride containing a dopant is exposed to heat at a temperature of 600°C or less. See the English abstract and figure 5.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to expose the group III nitride containing a dopant to heat at temperature of 600°C or less in the method of the applicant's admitted prior art because in doing so the optical characteristics of the device are improved without changing electrical characteristics. See the English abstract.

1. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this present application in view of Shih et

al. (US '320) and Isamu et al. (Japan 02257679) as applied to claims 25, 26, 27, 31, and 32 above, and further in view of Nagao (Japan 58100471).

The applicant's admitted prior art teaches forming the p-side electrode out of metal on the semiconductor layer, but fails to teach that the metal is aluminum as recited in present claims 28-30.

Nagao teaches a method of making a light-emitting diode in which the p-side electrode is made of aluminum. See the English abstract.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to form the p-side electrode from aluminum in the method of the applicant's admitted prior art because in doing the life and reliability of the device is improved. See the English abstract.

4. Claims 33, 34, 35, 36, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this present application in view of Shih et al. (US '320) and Isamu et al. (Japan 02257679).

The applicant's admitted prior art teaches a method for fabricating a semiconductor device, comprising the steps of (see col. 1, line 5 to col. 2, line 61 of the Background and figure 10 of the patent no. 6,117,700):

a) forming a semiconductor layer 104 of a group III nitride containing a dopant over a substrate 101, wherein the dopant includes magnesium (Mg), zinc (Zn), calcium (Ca), strontium (Sr), and beryllium (Be);

b) exposing the semiconductor layer to plasma at temperature, thereby making the conductivity type of semiconductor layer p-type;

c) after step b) forming a p-side electrode out of a metal on the semiconductor layer.

The applicant's admitted prior art teaches performing plasma heating after the formation of the semiconductor layer 104 of a group III nitride containing a

dopant, but fails to teach that the plasma heating is done in the presence nitrogen as recited in present claim 34.

Shih teaches a method of forming a semiconductor layer in which a semiconductor layer of a group III nitride containing a dopant is annealed by nitrogen plasma that is generated by RF. See the abstract.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to anneal the semiconductor layer 104 of a group III nitride containing a dopant by nitrogen plasma that is generated by RF in the method of the applicant's admitted prior art because in doing so the unwanted defects caused by high temperature process are prevented. See the abstract.

The applicant's admitted prior art teaches exposing the semiconductor layer to plasma for activating the p-type dopant at a temperature, but fails to teach annealing temperature range of 600°C or less as recited in present claims 33 and 36.

Isamu teaches a method of making a gallium nitride compound semiconductor light-emitting device in which a group III nitride containing a dopant is exposed to heat at a temperature of 600°C or less. See the English abstract and figure 5.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to expose the group III nitride containing a dopant to heat at temperature of 600°C or less in the method of the applicant's admitted prior art because in doing so the optical characteristics of the device are improved without changing electrical characteristics. See the English abstract.

The applicant's admitted prior art teaches exposing the semiconductor layer to plasma for activating the p-type dopant before the formation of the p-side but fails to teach exposing the semiconductor layer to plasma after the formation of the electrode as recited in present claim 37.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to expose the semiconductor layer to plasma for activating the p-type dopant after the formation of the p-side electrode because in the absence of new or unexpected results, the mere reversal of the order of performing process steps has been held to be prima facie obvious. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

5. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this present application in view of Isamu et al. (Japan 02257679).

The applicant's admitted prior art teaches a method for fabricating a semiconductor device, comprising the steps of (see col. 1, line 5 to col. 2, line 61 of the Background and figure 10 of the patent no. 6,117,700):

a) forming a semiconductor layer 104 of a group III nitride containing a dopant over a substrate 101, wherein the dopant includes magnesium (Mg), zinc (Zn), calcium (Ca), strontium (Sr), and beryllium (Be);

b) forming a p-side electrode out of a metal on the semiconductor layer, wherein the metal includes nickel and gold; and

c) exposing the semiconductor layer to plasma at temperature, thereby making the conductivity type of semiconductor layer p-type.

The applicant's admitted prior art teaches exposing the semiconductor layer to plasma for activating the p-type dopant at a temperature, but fails to teach annealing temperature range of 600°C or less as recited in present claim 39.

Isamu teaches a method of making a gallium nitride compound semiconductor light-emitting device in which a group III nitride containing a dopant is exposed to heat at a temperature of 600°C or less. See the English abstract and figure 5.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to expose the group III nitride containing a dopant to heat at temperature of 600°C or less in the method of the applicant's admitted prior art because in doing so the optical characteristics of the device are improved without changing electrical characteristics. See the English abstract.

2. Claims 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this present application in view of Isamu et al. (Japan 02257679) as applied to claims 39 and 40 above, and further in view of Nagao (Japan 58100471).

The applicant's admitted prior art teaches forming the p-side electrode out of metal on the semiconductor layer, but fails to teach that the metal is aluminum as recited in present claims 41-43.

Nagao teaches a method of making a light-emitting diode in which the p-side electrode is made of aluminum. See the English abstract.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to form the p-side electrode from aluminum in the method of the applicant's admitted prior art because in doing the life and reliability of the device is improved. See the English abstract.

Allowable Subject Matter

6. Claims 1-15 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092, the phone number after Jan 12, 2004 would be 571-272-1714. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918, the phone

number after Jan 12, 2004 would be 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-746-4082.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Long Pham
Primary Examiner
Art Unit 2814

L. P.